REMARKS

Claims 1, 3-9, 19-22 and 25-27 remain in this application. Claims 1 and 19 have been amended. Claims 22 and 27 have been cancelled. Claims 1 and 19 are independent claims.

In the Office action dated December 13, 2005, claims 19-22 and 27 were rejected under 35 U.S.C. 112, first paragraph, as allegedly failing to comply with the written description requirement. Claims 1, 3-6, 8, 9, 12, 14, 19, 20 and 22 were rejected under 35 U.S.C. 102(e) as allegedly being anticipated by McCormack et al. ("McCormack"). Claims 7, 15-18 and 21 were rejected under 35 U.S.C. 103(a) as allegedly being unpatentable over McCormack in view of Yiu. Claim 26 was rejected under 35 U.S.C. 103(a) over McCormack in view of Blazo et al. ("Blazo").

The Office action was made final. Applicants respectfully request reconsideration of the finality of the Office action. The Office action included new grounds of rejection, which were not necessitated by amendment. Specifically, page 2 of the Office action asserted that noncompliance with the written description requirement was the basis for the new grounds of rejection of claims. Moreover, MPEP 2163 specifically states that in order to reject a claim for lack of adequate written description, "the Examiner must set forth express findings of fact" and that these findings should (A) identify the claim limitation at issue, and (B) establish a *prima facie* case by providing reasons why a skilled person in the art would not have recognized that the inventor was in possession of the invention in view of the disclosure of the application as filed (with general allegations being insufficient). The Office action identifies the claim limitation at issue, but does not attempt to establish a *prima facie* case by providing any reasons.

Reconsideration of the finality of the rejection and reconsideration of the claims in view of the comments that will follow are both respectfully requested.

A. Propriety of a Final Rejection

MPEP 706.07(a) states that under present practice, second and any subsequent Office actions on the merits shall be final, except where the Examiner introduces a new ground of rejection that is neither necessitated by Applicant's amendment of the claims nor based on information submitted in

an information disclosure statement filed during the period set forth in 37 CFR 1.97(c).

In Applicants' previously filed amendment (mailed November 23, 2005), claim 27 was not amended. Nevertheless, the Office action presented the new grounds of rejecting claim 27 under 35 U.S.C. 112, first paragraph, as failing to comply with the written description requirement. Since the claim was not amended, it is clear that the previously filed amendment did not necessitate the new grounds of rejection.

Claim 19 was previously amended, but the feature of "jitter introduced by off-chip conditions" existed prior to the amendment. Nevertheless, it is this feature which was identified in the Office action as being in noncompliance with the written description requirement.

Since the new grounds for rejection was neither necessitated by Applicants' last amendment of the claims nor based on information submitted in an information disclosure statement, Applicants request that the finality of the Office action be removed for being premature.

B. *Prima Facie* Case of Noncompliance with the Written Description Requirement

MPEP 2163.04 states, "A description as filed is presumed to be adequate, unless or until sufficient evidence or reasoning to the contrary has been presented by the Examiner to rebut the presumption . . . The Examiner has the initial burden of presenting a preponderance of evidence why a person skilled in the art would not recognize in an Applicant's disclosure a description of the invention defined by the claims." This section of the MPEP also provides a statement of rejection requirements. It is stated that in rejecting a claim, the Examiner must set forth findings that include (A) identifying the claim limitation at issue, and (B) establishing a *prima facie* case by providing reasons why a person skilled in the art would not have recognized that the inventor was in possession of the invention as claimed in view of the disclosure of the application as filed.

The rejections based on 35 U.S.C. 112, first paragraph, are found on pages 10 and 11 of the Office action. While requirement (A) is satisfied, the Office action provides no reasons why a person skilled in the art would not have recognized that the inventors were in possession of the invention as claimed in view of the disclosure of the application as filed.

Consequently, Applicants respectfully assert that a proper rejection has not been presented. On page 2 of the Office action, it is asserted that Applicants' previously filed remarks with regard to "non-enablement" were moot in view of the new grounds of rejection. Applicants respectfully point out that the comments regarding "non-enablement" identified the portions of the application as filed that support the features which are now considered to be noncompliant with the written description requirement. Therefore, the remarks remain relevant, despite the presentation of the new grounds of rejection.

Applicants request an explanation of reasons why a person skilled in the art would not have recognized that the inventors were in possession of the invention, so that Applicants may then address the reasons.

C. Satisfaction of the Written Description Requirement with Regard to Claims 19-22

Claims 19-22 were rejected under 35 U.S.C. 112, first paragraph, as failing to comply with the written description requirement because the specification allegedly does not disclose that "the jitter is induced by off-chip conditions." Claim 19 describes a method of providing equalization for a crosspoint switch formed on an integrated circuit chip. The method includes providing on-chip measurements of jitter of electrical signals, wherein the jitter is induced by off-chip conditions. The invention described in method claim 19 is not one in which jitter is induced, but is instead one which includes providing on-chip measurements of the jitter induced by off-chip conditions and at least partially basing the setting of equalization circuitry on the on-chip measurement of jitter.

In paragraph [0009] on page 3 of the specification, it is stated that for the embodiment in which the crosspoint switch is formed as a single integrated circuit chip, the chip is often connected to a printed circuit board. With such a connection, an ordinarily skilled artisan would find it to be a fundamental understanding that "on-chip" actions are those actions which occur on the chip, while off-chip conditions are those conditions that are outside of the chip. Applicants are aware of no other understanding. In accordance with this basic understanding in the art, jitter that is generated as a result of conditions on the printed circuit board is jitter that is induced by off-chip conditions when the chip is connected to the printed circuit board.

Then, in paragraph [0028] on page 6 of the specification, it is stated that if the crosspoint switch is connected to a printed circuit board, each input equalization may be tailored to improve signal integrity over the circuit board trace (e.g., copper trace) of the associated input channel. Paragraph [0033] on page 8 of the specification states, "In accordance with the invention, the anticipated transmission losses experienced by signals received via input channel lines 32 and 34 are determined, so that the equalization circuitry 48 may be set to compensate for the losses." Similarly, on page 12, paragraph [0044] states that for the printed circuit board 86 of Fig. 5, the transmission loss for each channel to a crosspoint switch 88 is determined, as indicated at step 100 of Fig. 6. As shown in Fig. 5, the crosspoint switch 88 is an integrated circuit chip that is connected to the printed circuit board 86. In Fig. 5, a single copper trace 101 is included to show one connection of an input port to the first stage crosspoint switch 88. As described in paragraph [0044], there will be variations in the lengths of traces for the input channels to the first stage crosspoint switch and the distances that signals must travel from their sources to the different input ports will result in different signal losses.

The Office action does not assert that there is a lack of written description with regard to providing the on-chip measurements. The issue raised in the Office action is whether the specification discloses that "the jitter is induced by off-chip conditions." Since the lengths and other conditions of circuit board traces are "off-chip conditions," Applicants assert that the specification discloses this feature. Reconsideration of the rejection of claims 19-22 under Section 112, first paragraph, is requested.

D. Satisfaction of the Written Description Requirement with Regard to Claim 1

Claim 27 was rejected because the specification allegedly does not disclose that the equalization circuitry is configured to "recurringly execute said jitter measurement and recurringly execute responsive selection of said levels of equalization." Since the features of claim 27 have been incorporated into claim 1, the rejection will be addressed with respect to the amended independent claim.

It is respectfully asserted that the specification as originally filed discloses recurring execution of measurements and recurring executions of

selections of equalization. While not all of the embodiments described in the specification provide configuration as set forth in amended claim 1, the automated embodiments are described as enabling this configuration. On page 3 of the specification, paragraph [0010] describes the adaptive equalization embodiment as one in which equalization settings are varied automatically, providing the advantage in which the level of equalization can track changes in the environment or in the supported hardware. The description is consistent with that of amended claim 1, which concludes with the clause, "thereby enabling said levels of equalization to track variations in said transmission losses." The level of equalization can track changes in the environment or in the supported hardware only if the measurements detect that a change in the environment or the supported hardware has occurred since a previous measurement. Given the description in paragraph [0010], a person reasonably skilled in the art would recognize that Applicants had possession of the claimed invention at the time that the application was filed.

Moreover, the last sentence in paragraph [0033] on page 8 of the specification states that a practical alternative to measuring transmission loss is to repeatedly adjust the equalization while monitoring the output jitter, and then select the equalization setting that provides the best results. Since the equalization is repeatedly adjusted and the output jitter is monitored as the levels of equalization are repeatedly adjusted, paragraph [0033] provides description of the feature which has been added to claim 1.

Paragraph [0049] on pages 13 and 14 of the specification compare the adaptive equalization embodiment to the other embodiments of crosspoint switches described in the application. The adaptive equalization automatically adjusts the equalization setting so that it has an advantage over the adjustable equalization embodiment. Moreover, adaptive equalization tracks changes in the environment. While changes in temperature, IC processing, and supply voltages may have only a minimal effect on the optimal equalization setting, the automated adaptive equalization embodiment follows the effect to be eliminated. While the adjustable equalization embodiment operates well within its single setting, the adaptive equalization embodiment enables tracking of one-setting differences in equalization level without requiring the user to periodically check jitter. This is possible, since the adaptive equalization embodiment provides the periodic jitter checking described in amended claim 1.

Reconsideration of the feature added to claim 1 by amendment is respectfully requested.

E. Patentability of Amended Claim 1

Claims 1, 3-6, 8, 9, 12, 14, 19, 20, 22 and 27 were rejected under 35 U.S.C. 102(e) as allegedly being anticipated by McCormack. In order to place the claim in a better condition for appeal, claim 1 has been amended to incorporate the features of claim 27.

Claim 1 describes the equalization circuitry of the crosspoint switch integrated circuit as being configured to measure jitter and to utilize the jitter measurements as the basis for offsetting transmission losses. In the portion of the Office action entitled "Response to Arguments," it is stated on page 3 that the crosspoint switch integrated circuit of McCormack anticipates equalization circuitry configured to measure jitter within electrical signals. The Office action cites block 201 in Fig. 1 of McCormack, paragraph [0008] on page 1, paragraph [0037] on page 2, and paragraph [0054] on page 4 of McCormack. The same portions of McCormack are cited on page 12 of the Office action. Applicants respectfully assert that these portions do not teach a crosspoint switch integrated circuit having equalization circuitry configured to measure jitter.

Block 201 in Fig. 1 merely shows a rectangle. There is no indication that the block has the capability of providing measurements of any type. The third cited portion of McCormack (paragraph [0037]) refers to block 201. It is stated that block 201 represents input signal equalization circuits. The input equalization circuits are coupled to the switch core of the crosspoint integrated circuit of Fig. 1. Persons skilled in the art would readily recognize that "input signal equalization circuits" are equalization circuits that provide equalization for input signals. Nothing within paragraph [0037] indicates that the input signal equalization circuits generate measurements. It follows that neither Fig. 1 nor paragraph [0037] provides a *prima facie* case of anticipation with respect to a crosspoint switch integrated circuit having equalization circuitry configured to measure jitter.

Similarly, paragraph [0008] in McCormack does not teach a crosspoint switch integrated circuit having equalization circuitry configured to provide measurements. There is no reference to generating measurements in paragraph [0008]. Rather, this paragraph on page 1 of McCormack defines inter-symbol interference (ISI). It is stated that ISI can result when the bandwidth of a transmission media or an amplifier circuit is not sufficient to pass the frequency content of a data signal without attenuating or phase-shifting some of the constituent frequencies such that a data pulse will not reach its

full amplitude. When the data pulse passes a given threshold level, a pattern-dependent jitter occurs. Paragraph [0008] states that this jitter is often due to the narrowing or widening of the data pulses that depend on the voltage history. The paragraph provides no description of measurements.

The final citation in the Office action with respect to *prima facie* anticipation is paragraph [0054] on page 4 of McCormack. Again, there is no reference to generating measurements within the equalization circuitry. That is, paragraph [0054] does not anticipate equalization circuitry configured to measure jitter and to use the jitter measurements. The paragraph in McCormack merely refers to passive elements. These passive elements can be segmented or programmable (i.e., tunable). For instance, the upper metal layers of an integrated circuit can be changed to allow easy tuning of a circuit's ISI jitter characteristics.

It is well settled that a rejection under Section 102 requires that each feature of a claim be shown to exist within a single prior art reference. None of the four citations to teachings of McCormack provides a *prima facie* case of anticipation with respect to a crosspoint integrated circuit having equalization circuitry configured to measure jitter within electrical signals and to utilize the jitter measurements as the basis for offsetting transmission losses. Four portions of McCormack were cited in the Office action, but none refers to generating measures of jitter. Paragraph [0054] refers to passive elements that can be tunable to offset jitter. But the passive elements do not generate measures of jitter which may then be used as the basis for offsetting transmission losses. Fig. 2 of McCormack shows a network (21) with passive elements. The network provides pre-compensation. The network is not described as being one in which measures of jitter are generated. The network (21) of Fig. 2 does not show "active" elements. The passive elements do not include the capability of generating measurements.

On pages 8 and 9 of the Office action, the remarks made by Applicants with regard to the patentability of claim 27 were addressed. As noted above, the features of claim 27 have been incorporated into claim 1. Thus, claim 1 now states that the equalization circuitry is configured to recurringly execute jitter measurements. The Office action cites block 21 in Fig. 2 of McCormack, as well as Fig. 4 and paragraphs [0054] to [0057]. Applicants do not dispute that McCormack teaches that a network of passive elements may be tunable. For example, the network of resistors and capacitors in Fig. 2 may be tunable. However, none of the elements shown in Fig. 2 or Fig. 4 of McCormack provides the capability of recurringly executing

jitter measurements which are used as the basis for offsetting transmission losses. Applicants respectfully point out that radios and televisions are tunable, but under ordinary circumstances it is the decision process of users that is the basis for tuning a radio or television. Similarly, the tunability of block 21 in Fig. 2 does not in any way anticipate, teach or suggest that the network is configured to measure jitter. If it is the position of the Examiner that circuits that are tunable inherently generate measurements that are then used as the basis for tuning, Applicants request support for this conclusion of inherency.

The Office action includes the entirety of paragraphs [0056] and [0057] of McCormack. The first of these paragraphs merely identifies the connection of components. Input transmission lines are coupled to the network shown in Fig. 2. There is no reference to circuitry that is configured to recurringly execute jitter measurements. In paragraph [0057], there is another reference to the ability to tune circuitry. However, there is no description of the same circuitry being able to execute jitter measurements that are then used as the basis for tuning. Again, unless it is the position of the Examiner that coupling and decoupling capacitors to provide tuning inherently includes the execution of jitter measurements, less than all of the features of the combination of claims 1 and 27 have been addressed in the Office action. On the other hand, if it is the position of the Examiner that all circuits that are tunable inherently execute measuring, Applicants request support for this conclusion of inherency.

F. Patentability of Amended Claim 19

Claim 19 describes a method of providing equalization for a crosspoint switch formed on an integrated circuit chip. The method comprises determining signal characteristics, including providing on-chip measurements of jitter. The method further comprises setting equalization circuitry, with the setting be automated, adaptive, and at least partially based on the on-chip measurements of jitter.

As with claim 1, it appears that the rejection of claim 19 is based upon inherency. The Office action refers to the ability to tune a circuit, but the cited portions of McCormack do not anticipate, teach or suggest providing on-chip measurements of jitter. Applicants again respectfully refer to tuning of a radio or television. While the radio or television is tunable, the setting is not necessarily automated and the tuning is not based upon "on-chip"

measurements. Rather, the tuning of a radio or television is based upon the decision making and the actions of a user.

In rejecting claim 19, the Office action asserts that McCormack teaches providing on-chip measurements of jitter of electrical signals. The portions of McCormack that are cited for supporting this conclusion are (a) Fig. 2, block 21, (b) page 1, paragraph [0011], and (c) page 4, paragraphs [0051] to [0060]. Referring firstly to block 21 in Fig. 2, only resistors and capacitors are shown. The combination of resistors and capacitors provides pre-compensation for signals. The drawing provides no basis for concluding that the pre-compensation network provides on-chip measurements of jitter.

Nor does paragraph [0011] on page 1 of McCormack provide support for the conclusion that McCormack teaches on-chip measurements of jitter. This paragraph merely states that one conventional approach for mitigating ISI in linear transmission media is static or adaptive equalization. In static or adaptive equalization, a circuit which inverts the characteristics of the media is placed at the receiver to produce a facsimile of the original signal. Neither on-chip measurements nor off-chip measurements are considered in this paragraph.

Thus, a *prima facie* case of anticipation is present only if the on-chip measurements are described in paragraphs [0051] to [0056] on page 4 of McCormack. Paragraph [0051] merely refers to the component values of series capacitors and resistors. The paragraph states that the component values of the capacitors are pre-selected, such that the impedance of the capacitors equals the resistance value RS approximately at the corner frequency of the amplifier chain. This teaching regarding pre-selection leads away from the claimed invention, which includes automated and adaptive equalization circuitry, with the setting being at least partially based on on-chip measurements of jitter. Paragraph [0052] states that the network may be used with a modest ratio of high to low frequency gain. This provides no basis for anticipation of claim 19 under Section 102. Paragraph [0053] is similar to [0051] with respect to leading away from the invention described in claim 19. Paragraph [0053] states that the network may be applied externally to the integrated circuit in order to remove ISI already in prefabricated circuits. That is, the teachings of this paragraph are that there are benefits to providing the equalization off-chip, rather than in the manner described in claim 19.

Turning to paragraph [0054], this paragraph describes tunability. However, there is no description of the ability to provide measurements.

Since a network that enables tuning does not inherently generate measurements, this paragraph does not anticipate the claimed feature of providing on-chip measurements of jitter.

In paragraph [0055] of McCormack, it is stated that the network may be placed between cascaded crosspoint switch devices so as to reduce signal degradation. One difference between the invention described in claim 19 and the teachings of paragraph [0055] is that the equalization of the claimed invention occurs within equalization circuitry housed within the crosspoint switch, rather than between a pair of crosspoint switch devices. A second difference is that the invention of claim 19 provides on-chip measuring, while paragraph [0055] does not describe measuring.

The final paragraph cited in the Office action is paragraph [0056] of McCormack. This portion of the prior art reference merely describes connections. There is no reference to measurements.

Since the prior art reference to McCormack does not anticipate on-chip measurements of jitter, the reference does not provide a *prima facie* case of anticipation under Section 102. Reconsideration of the claim and its dependent claims is requested.

G. "Changing Upper Metal Layers of an Integrated Circuit"

The Office action relies upon paragraph [0054] on page 4 of McCormack for the conclusion that the responsive selection of levels of equalization can be executed recurringly. This feature was previously contained within claim 27, but has been added to claim 1 by amendment.

The teachings of a prior art reference must be considered in view of what would be understood by a person of ordinary skill in the particular art. Here, a person of ordinary skill in the art of a crosspoint switch integrated circuit would readily recognize that in view of the dimensions of integrated circuits, changing upper metal layers of such a circuit would not be an action that could occur recurringly, given modern technology. One possible explanation for the teachings of paragraph [0054] is that at the fabrication stage of an integrated circuit, the upper metal layer may be designed on the basis of the intended application. If the intended application is known, the ISI jitter characteristics can be identified or estimated. Another possibility is that the upper metal layers are changed in a one-time manner, such as with volatile memory in which metal is used in the same manner as a "fuse" to provide permanent changes.

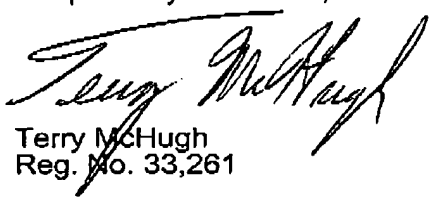
If it is the position of the Examiner that another explanation is plausible, Applicants respectfully request that the explanation be identified. Reconsideration is requested.

H. Teachings of Yiu and Blazo

The patents to Yiu and Blazo were cited for features contained within dependent claims. Remarks provided with the previous amendment are incorporated herein by reference. Yiu was cited for its teachings regarding switchable connections that are arranged in electrical parallel, with components that include inductors and resistors. It is not asserted in the Office action that Yiu renders it obvious to modify the teachings of McCormack et al. to include on-chip jitter measurements and to include equalization circuitry that achieves automatic selections of levels of equalization in response to the on-chip jitter measurements. Blazo was cited for its teachings regarding particular elements of a jitter measurement capability. Neither Blazo nor McCormack teaches or suggests providing a crosspoint switch integrated circuit having a jitter measurement component of any type. Moreover, neither reference provides the description or suggestion of a multiplexer used in the manner described in claim 25 with respect to equalization circuitry of a crosspoint switch integrated circuit.

Applicants respectfully request reconsideration of the claims in view of the amendments and remarks made herein. A notice of allowance is earnestly solicited. In the case that any issues regarding this application can be resolved expeditiously via a telephone conversation, Applicants invite the Examiner to call Terry McHugh at (650) 969-8458.

Respectfully submitted,



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